



SIGNAL INTEGRITY

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Intentional clock modulation

An ideal digital clock, from the standpoint of system timing, is an infinite succession of very fast-edged, identical pulses with a perfectly repeating structure. Unfortunately, from an electromagnetic-compatibility (EMC) perspective, such a clock is also the worst of all possible signals because it radiates like crazy. In polite engineering circles, this situation is calmly referred to as a "fundamental trade-off." Late at night, when we engineers let our hair down, I've heard other terms used to describe it.

The problem with a simple, repetitive signal, such as a clock, is that all its spectral power can become concentrated at a relatively small number of discrete frequencies. When these discrete frequencies leak out of your product's packaging and into the outside world, all the radiated clock power is concentrated in a small number of radiated modes.

Data signals don't have this problem. Random data signals spread their spectral power among a much larger number of radiated modes, each mode having a smaller average power. Less power in each mode is better, because both FCC and EN emissions regulations are written to penalize the worst-case (peak) radiation in any given mode.

Although the data nets in your product undoubtedly radiate more total power than the clocks, they usually contribute less to the FCC/EN peak-radiation measurements, because the radiation from the data nets is spread more evenly and at a relatively low level across the vast territory of the electromagnetic spectrum.

Over the years, various techniques have been proposed for modulating, or dithering, the clock frequency to break up the accumulated spectral power into a larger number of new modes, each mode with a reduced energy content. If the new modes are separated from each other by more than 100 kHz—which is the effective bandwidth used for FCC/EN spectral-power measurements—the peak power measured within each 100-kHz band is reduced. Such proposals are usually backed by solid theoretical reasoning, and, for the most part, they are technically sound. Modulating the clock really does reduce the peak measured radiation. Unfortunately, the practical realization of this technique comes at a very high cost. You may gain a proper appreciation of the architectural cost of a modulated clock by considering a clock's many uses.

First and foremost, the clock directs the synchronous neural firings of your product's digital brain. When working with a purely digital product architecture, you might conclude that you need merely to guarantee a minimum clock period. Any modulation or dither above and beyond the minimum period should, theoretically, have no impact on the correctness of the computed results. Dither may perturb the timing of the final result (it is always slower than if you had run the machine continuously at full speed), but it should not affect the correctness—that's the theory.

On the practical side, intentional clock modulation of any kind complicates the attachment of your prod-

uct to any form of truly synchronous logic. For example, you can never use a modulated clock as the reference-clock input to an advanced data-communication transceiver (Ethernet, Fibre Channel, FDDI, ATM, SONET, or ADSL). These parts require a pristine, jitter-free reference clock. When connected to a jittery clock, these transceivers may fail to lock, or lock poorly, leading to data errors or other flaky behavior. Never use an intentionally modulated clock as the reference input for any kind of data-communication transceiver.

For similar reasons, you'll find a modulated clock unsuitable for any modern high-performance CPU. The latest CPUs all contain clock-multiplier circuits (PLLs), which are very sensitive to jitter in the coming reference clock. The Semiconductor Industry Association road map (www.semtech.org/public/roadmap/index.htm) implies that more and more components will incorporate clock multipliers in future years. This trend is one you won't want to forgo.

Finally, if you still favor clock modulation, wireless communication is becoming progressively more important in many applications. Modulated clocks should not be used as a reference source for RF-communication systems. For direct-sequence spread-spectrum links, especially those in which the data rate and the communications-modulation rate (the chip rate) are related by a fixed integer, it is important to have a stable, jitter-free system clock for the transfer of data to and from the RF subsystem.

In each of the three cases I've outlined here, it is, of course, still possible to connect your jittery main clock domain to a purely synchronous subsystem. This connection requires at least one clean reference clock for the synchronous side of your product (in addition to the modulated clock you already have), plus a dual-ported asynchronous FIFO to connect the modulated clock domain to the jitter-free domain. Why bother with this sort of architecture?

In this author's opinion, if control of EMC is your objective, you will be better served by any combination of the following techniques:

- Using solid power and ground planes in your pc board
- Minimizing the trace-to-plane spacing
- Using thin packages, close to the board
- Slowing the rise/fall time of the clock driver
- Using differential clock transmission
- Using a lower voltage clock, such as LVDS or GTL

Any of these techniques deliver the clock you need at a cost you can afford. **EDN**

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Intentional clock modulation complicates your product.